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HSF Property: ROHS

ACER_BAP31U

MAIN BOARD

2009.05.13

Wednesday, May 20, 2009		A01
DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE	INVENTEC			
DRAWER					TITLE ACER_BAP31U			
DESIGN								
CHECK								
RESPONSIBLE								
SIZE:					I VER:			
FILE NAME: XXXXXXXXXXX-XX					SIZE	CODE	DOC NUMBER	REV
P/N	XXXXXXXXXXXX				C	AX1	D-CS-1310A2264501-ALG	A01
					SHEET		1 of 35	

1. Schematic Page Description :

Montevina Schematic Ver : A02

1. Title

2. Schematic Page DESCR

3. Block Diagram

4. Annotations

5. Schematic Modify

6. Timing Diagram

7. Power Block Diagram

8. Adaptor in/Charge

9. 5VLA/5VA/3VA

10. 3VS/5VS/1.5V (DDR3)

11. 1.05VS/1.5S/1.8V/1.5VA

12. Power Latch/1.5VS/SCREW HOLE

13. CPU Core Power

14. GPU Core Power

15. Penryn Processor(1/2)

16. Penryn Processor(2/2)

17. CPU Thermal
18. Cantiga Host(1/6)

19. Cantiga DMI/Graph(2/6)

20. Cantiga DDRII(3/6)

21. Cantiga Power(4/6)

22. Cantiga Power(5/6)

23. Cantiga Ground(6/6)

24. Clock Generator

25. DDR3 SDRAM SO-DIMM0

26. DDR3 SDRAM SO-DIMM1

27. ICH9M CPU/IDE/SATA(1/4)

28. ICH9M PCI/PCIE/DMI/USB(2/4)

29. ICH9M GPIO(3/4)

30. ICH9M Power/GND(4/4)

31. LCD CNN/SATA/3G/WLAN

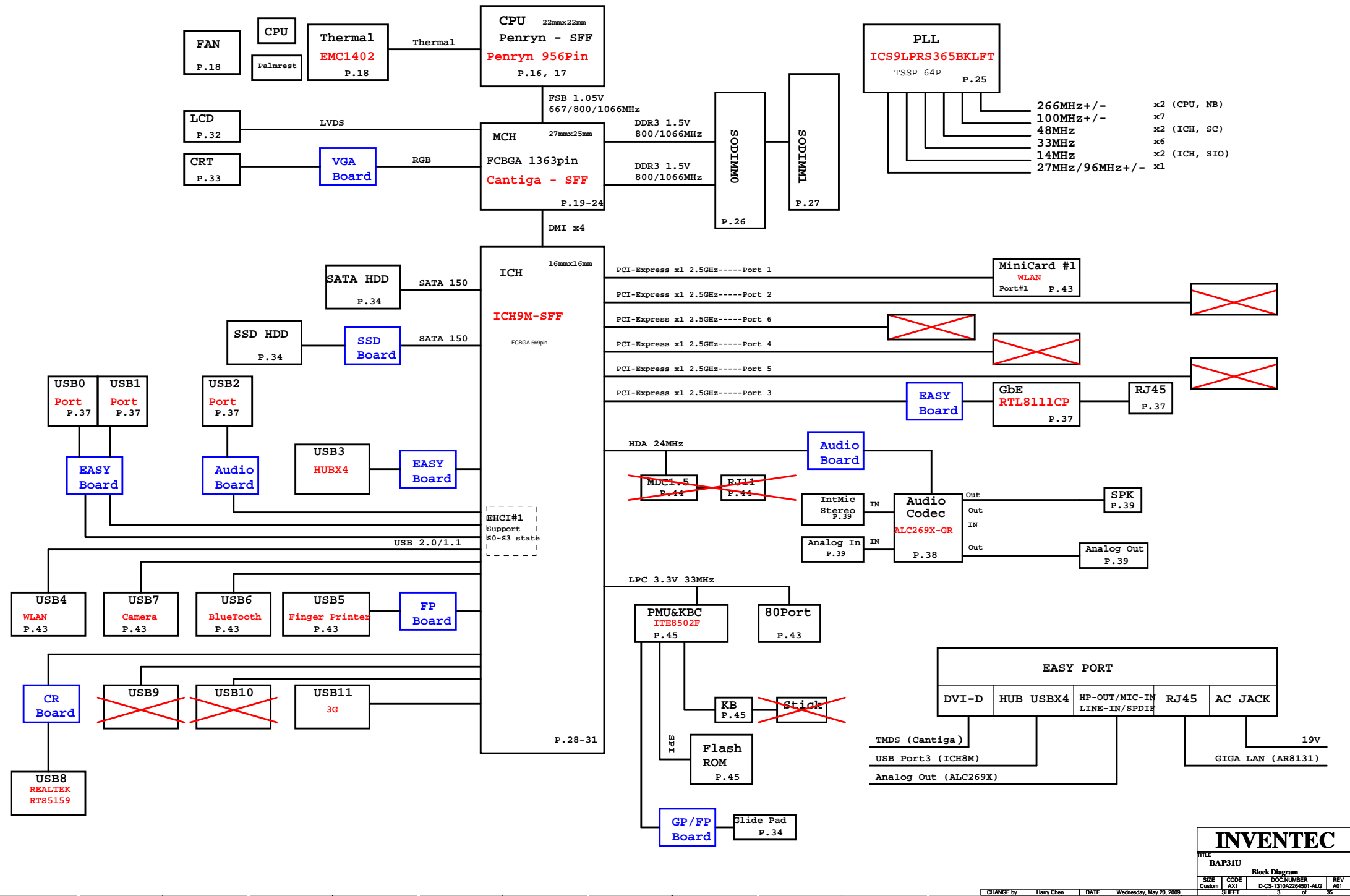
32. KBC ITE8512F

33. IO CN

34. IO CN

35. AUDIO CODEC

3. Block Diagram :



4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R

VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI;PCIE;DDRIII DLLs for GMCH/Core;PCIE for ICH9m by SLP_S3#_3R

+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

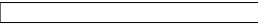



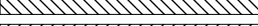



C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal
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5. Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Stripline Layer
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side, Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

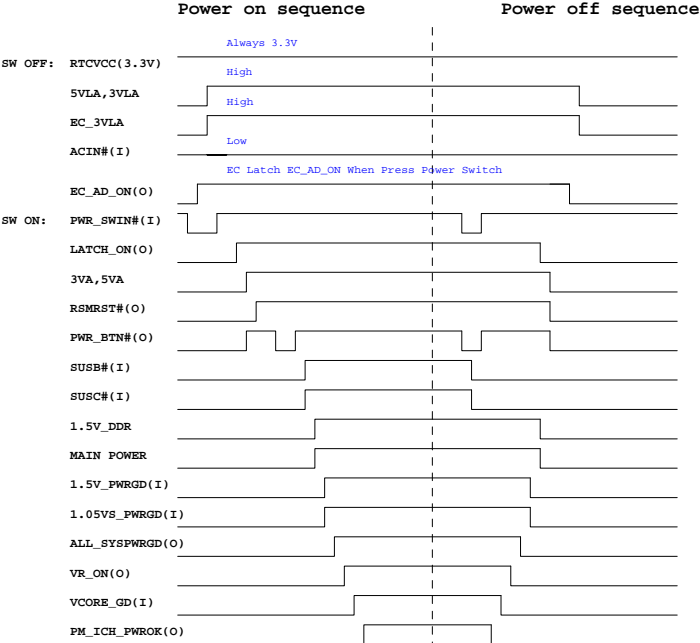
Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn SFF HFM: LFM:	1.3319V-1.4375V-1.4591V 0.9221V-0.9625V-0.9739V	18A
1.05VS	Penryn SFF : AGTL+ termination Cantiga GS: Core Cantiga GS: PCIE Cantiga GS:Core+IMEL+HSIO Cantiga GS:VCC_GMCH Cantiga GS:VCCA_SM_CK and NCTF Cantiga GS:VCC_DMI Cantiga GS:VCCA_SM Cantiga GS:VTT ICH9M:VCC1_05 ICH9M:DMI ICH9M:CPU_IO	1V-1.05V-1.10V 0.997V-1.05V-1.102V 0.9975V-1.05V-1.1025V 0.9975V-1.05V-1.1025V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V	4.5A 8.7A 1.78A 2.898A 10.154A 37.95mA 456mA 747.5mA 852mA 1.634A 48mA 2mA
1.5VS	Penryn SFF PLL Cantiga GS: QDAC Cantiga GS: LVDS Cantiga GS: TVDAC Cantiga GS: Various PLLS analog supply Cantiga GS: VCC_SM_CK Cantiga GS: VCC_SM ICH9M:PCIE_ICH ICH9M:SATA_ICH ICH9M:VCC_GLAN Mini Card: Express Card:	1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.71V-1.8V-1.89V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V	130mA 0.5mA 60.31mA 35mA 485mA 149.5mA 3.1625A 646mA 1.342A 80mA 650mA
1.5V	Cantiga GS: DDRIII System Memory	1.425V-1.5V-1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII:DDRIII Terminator:	0.7125V-0.75V-0.7875V	1.0A
3VS	Cantiga GS: HV CMOS Cantiga GS: VCCS_TVDCAC ICH9M:VCC3_3 ICH9M:VCCGLAN3_3 Thermal Sensor: Mini Card: UMTS Express Card: CLK Generator: ICS9LPRS365BKLFT Mini Card: WirelessLan Bluetooth: Super I/O: IT8305E Azalia Codec: ALC262 Azalia MDC:	3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V	105.3mA 78mA 308mA 1mA 5mA 1.3A 500mA
1.8VS	DVI	3.0V-3.3V-3.6V	120mA
3VA	ICH9M: RTC ICH9M:VCCSUS3_3 ICH9M:VCCCL3_3 ICH9M:VCCLAN3_3 LCD: Lan:AR8131 Azalia MDC: Flash ROM: BIOS	2V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V	6uA 212mA 73mA 78mA 2A 1A
5VS	Cardreader: RTS5159 Azalia Codec: ALC269 HDD: SATA ODD: SATA Audio AMP: G1432 Inverter: WebCam	3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA Max: 1.5A ; R/W: 900mA ; STDBY: 45mA
5VA	USB: x 2 ports USB	5VA 5VA	1A 2A 1.5A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V-3.3V-3.6V	300mA

6.Schematic modify Item and History :

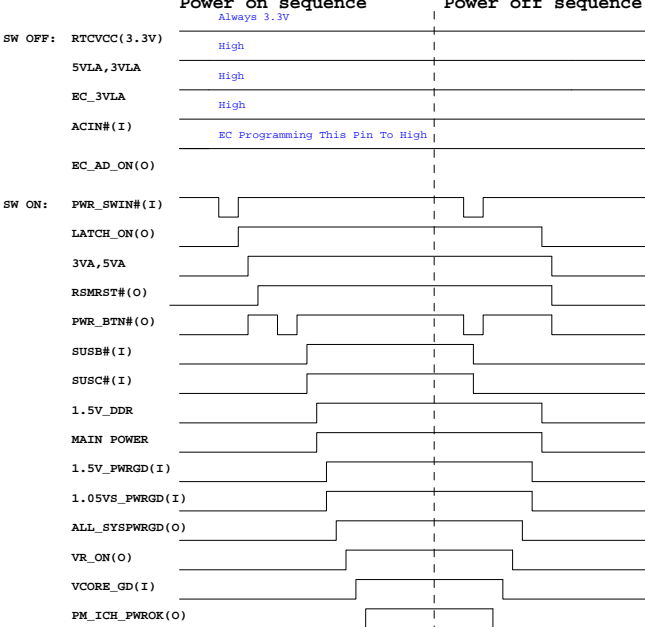
INVENTEC			
TITLE BAP31U			
Schematic Modify			
SIZE Custom	CODE AX1	DOC NUMBER D-CS-1310A2284501-ALG	REV A01

SYSTEM POWER ON/OFF SEQUENCE

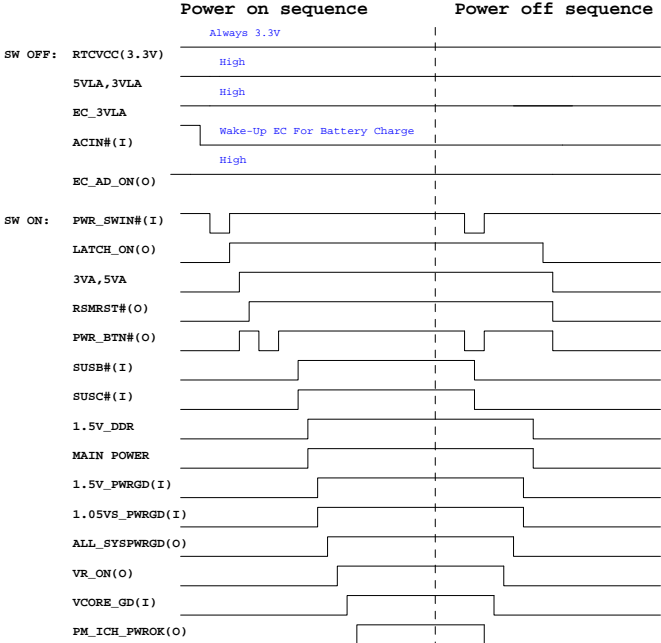
Power on/off sequence AC insert (without Battery Pack)



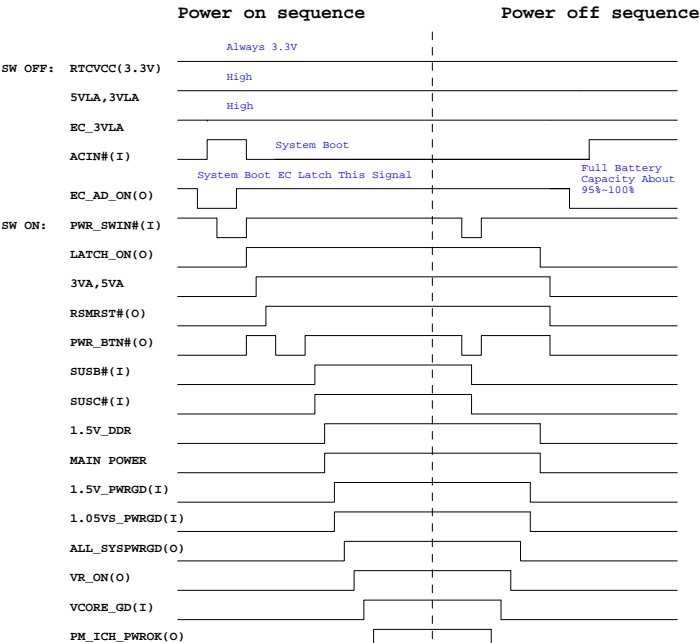
Power on/off sequence Battery insert (without AC adapter)



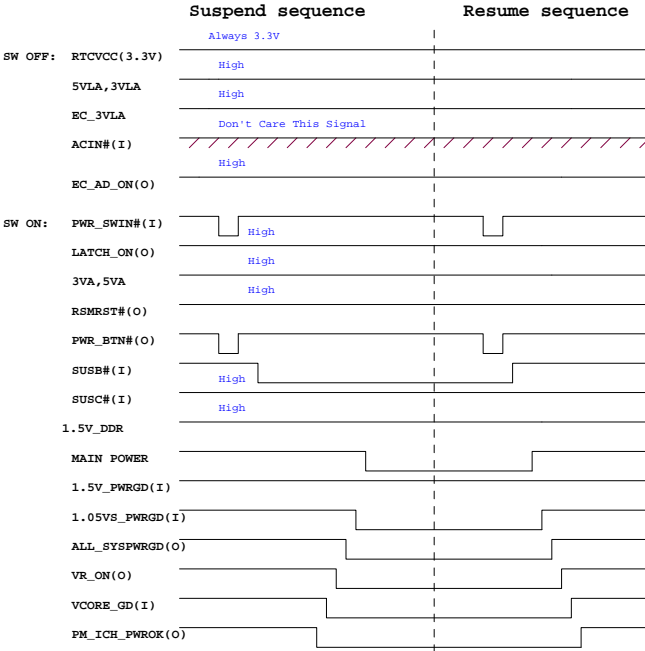
Power on/off sequence AC insert(with charge over 95%)



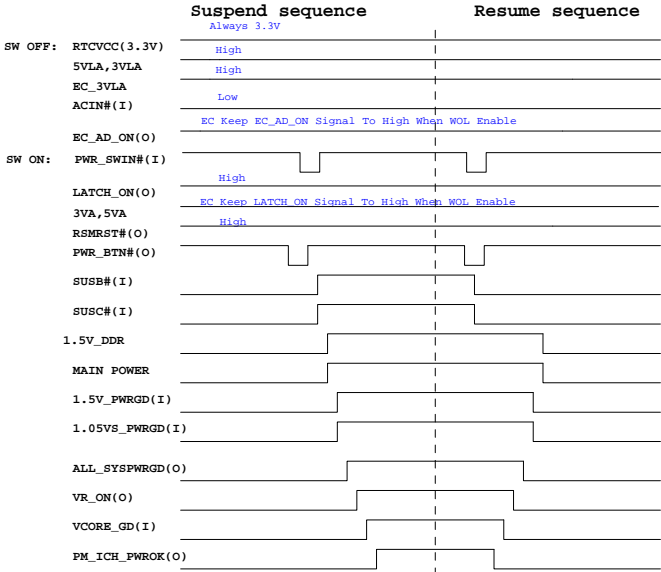
Power on/off sequence AC insert(without charge over 95%)



Suspend And Resume Sequence (S3)



Power on/off sequence after windows shoutdown (WOL enable)



INVENTEC

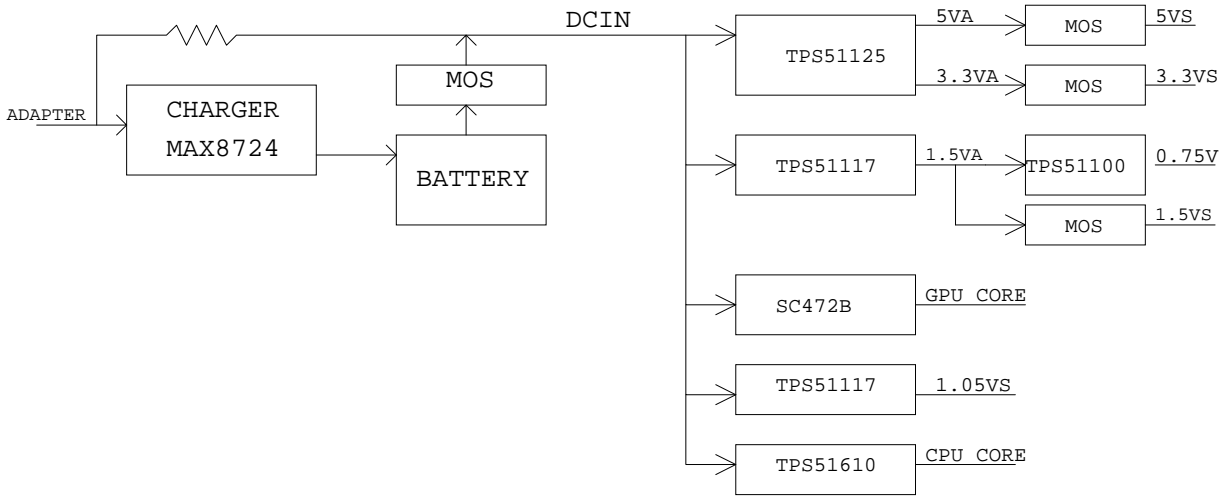
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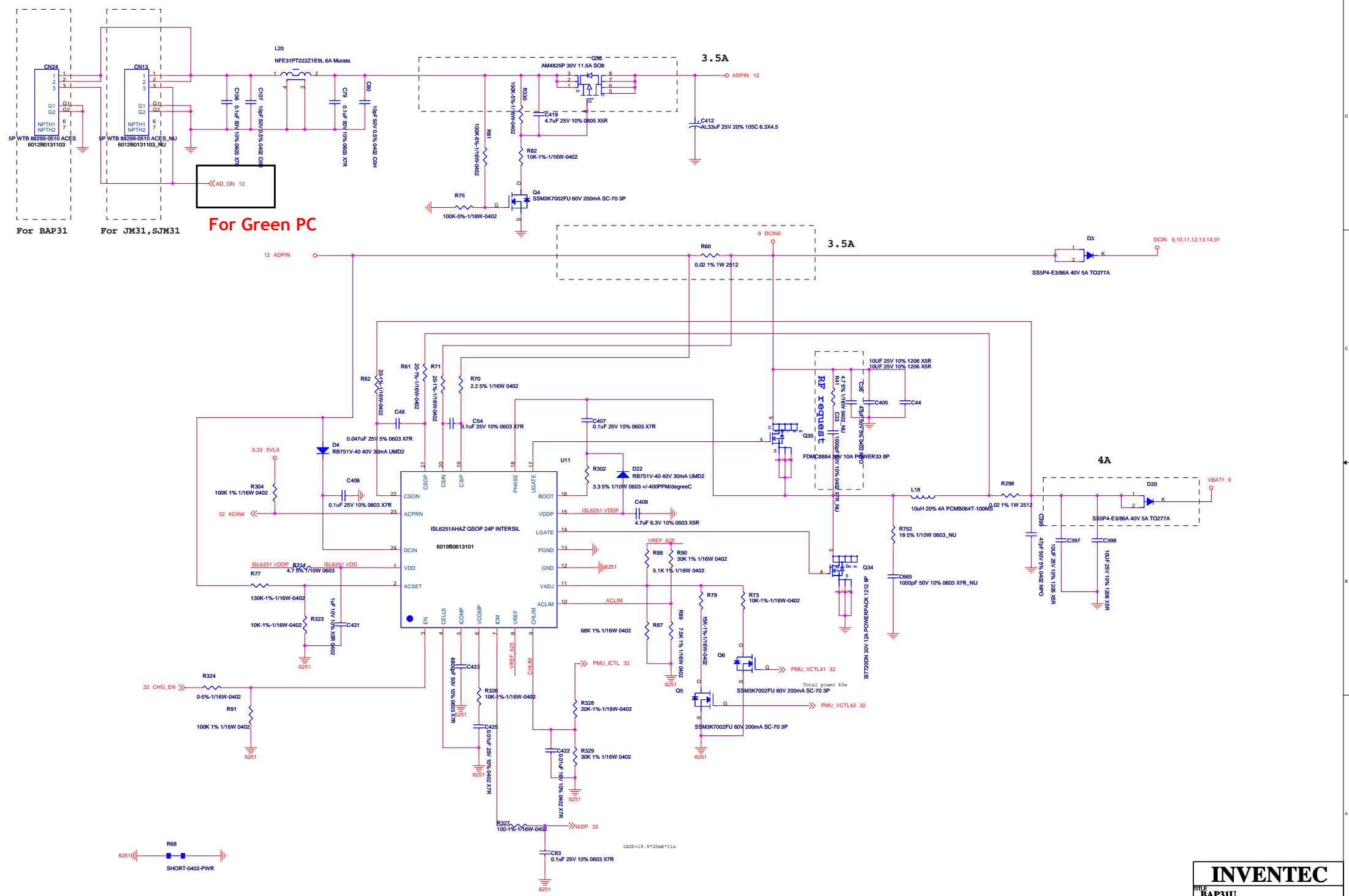
Time Diagram

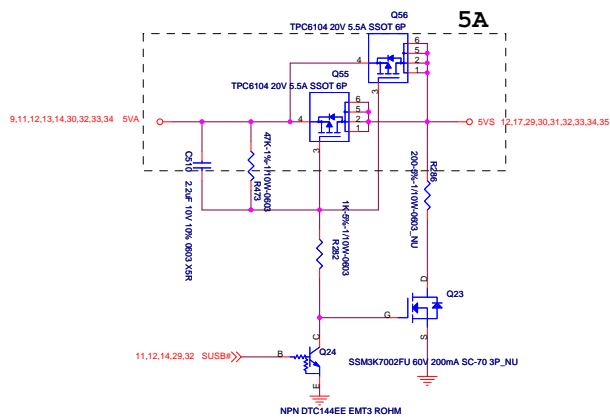
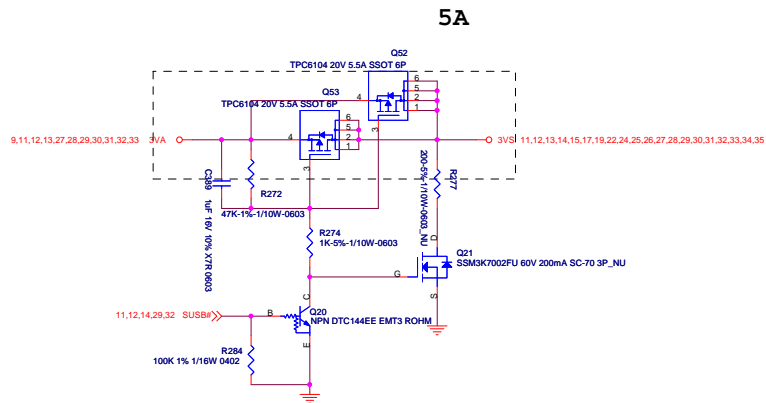
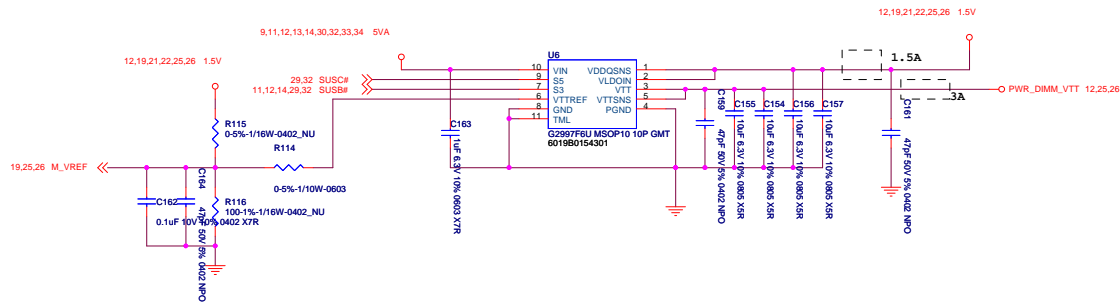
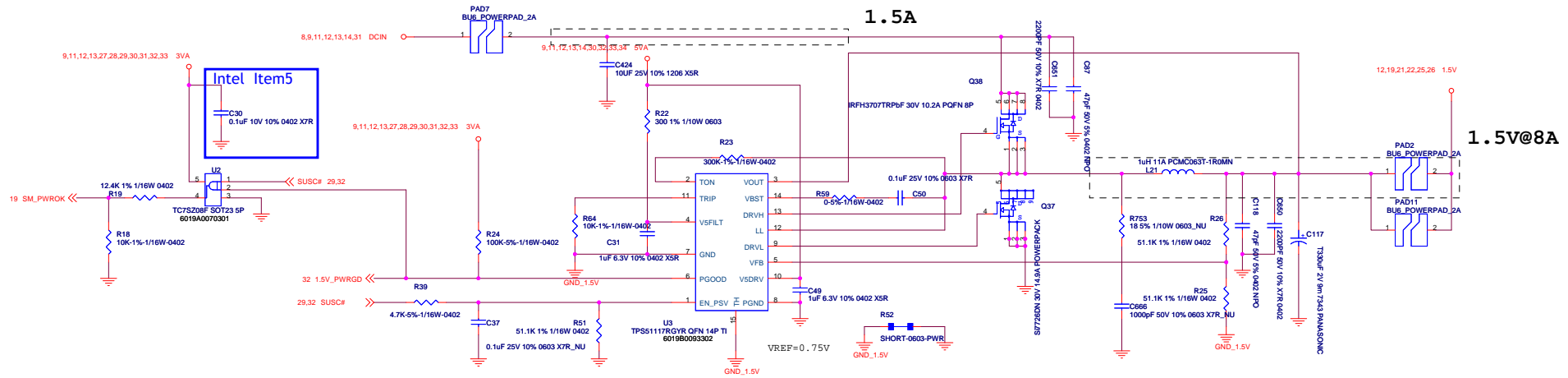
SIZE	CODE	DOC NUMBER	REV
Custom	AX1	D-CS-1310A264501-ALG	A01

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Power Block Diagram :

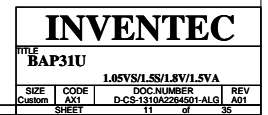
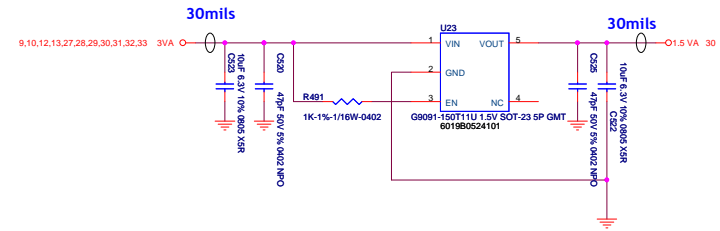


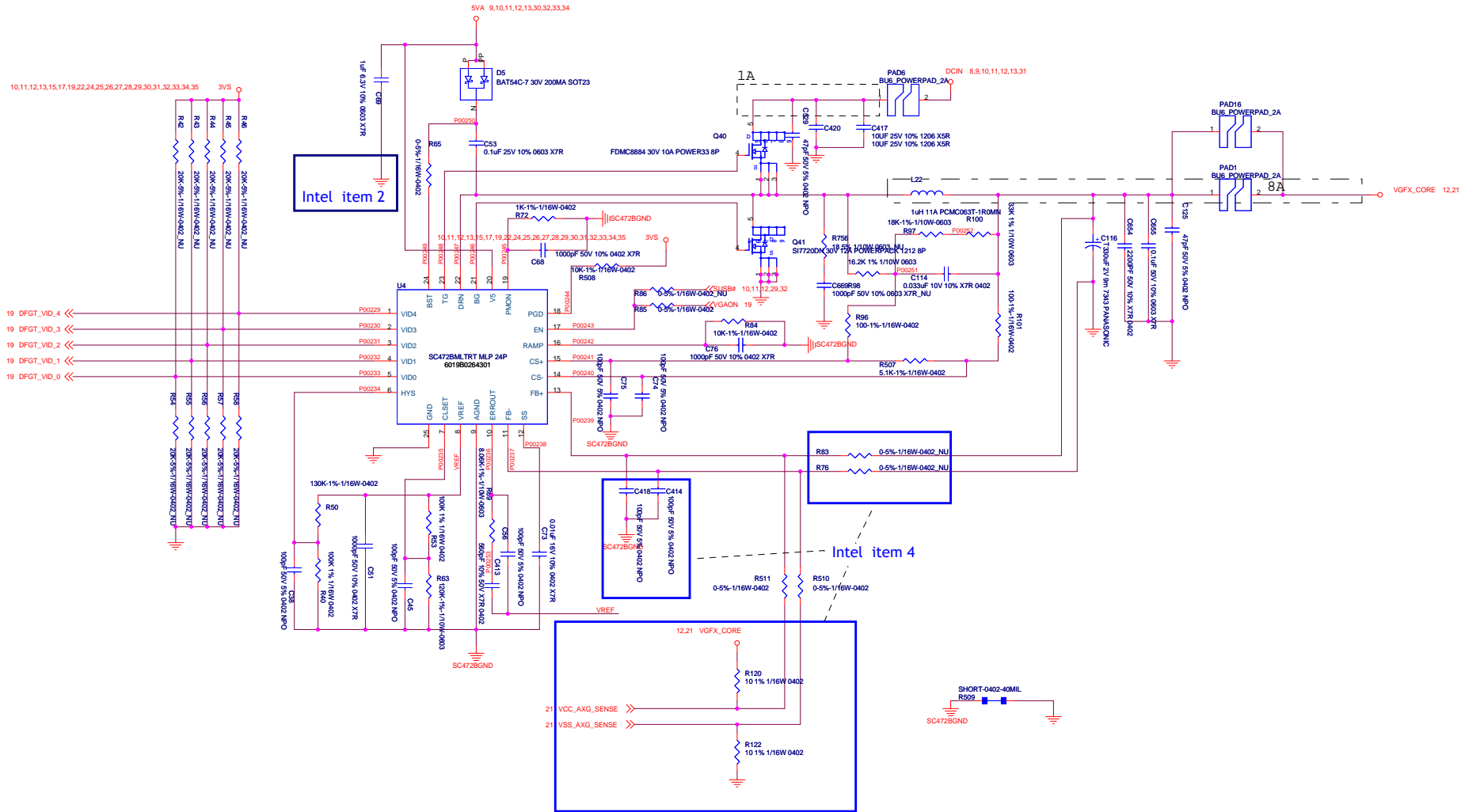




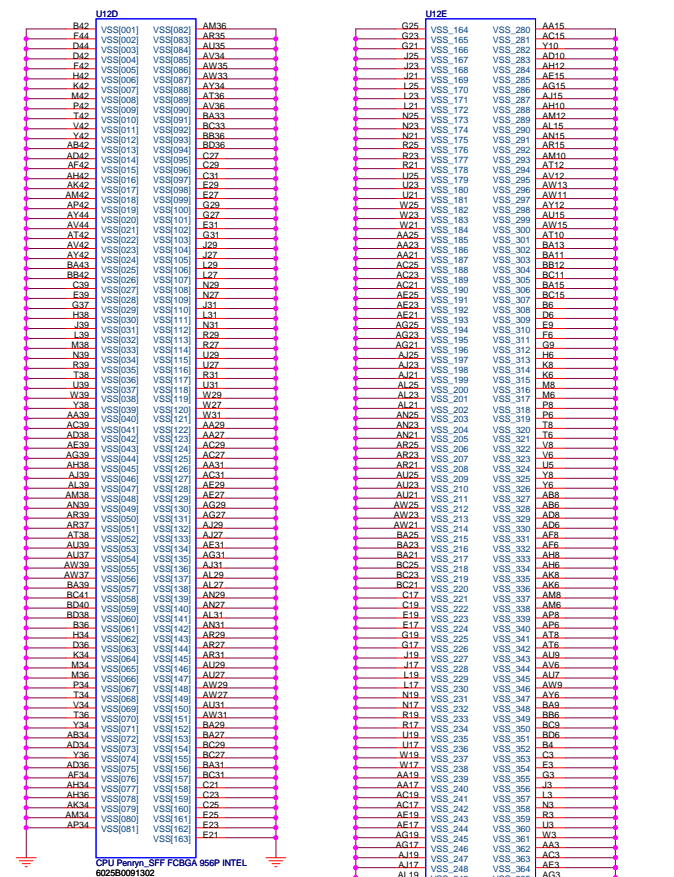
INVENTEC				
TITLE BAP31U				
3VS/5VS/1.5V (DDR3)				
SIZE	CODE	DOC NUMBER	REV	
Custom	AX1	D-C8-1310A2264501-ALG	A01	
SHEET			19 of 35	

CHANGE by: Harry Chen DATE: Wednesday, May 20, 2009

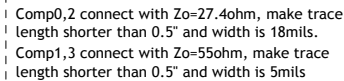




INVENTEC			
BAP31U			
GPU CORE			
SIZE	CODE	DOC NUMBER	REV
Custom	AX1	D-CS-1310A2284501-ALG	A01
SHEET	14	d	35

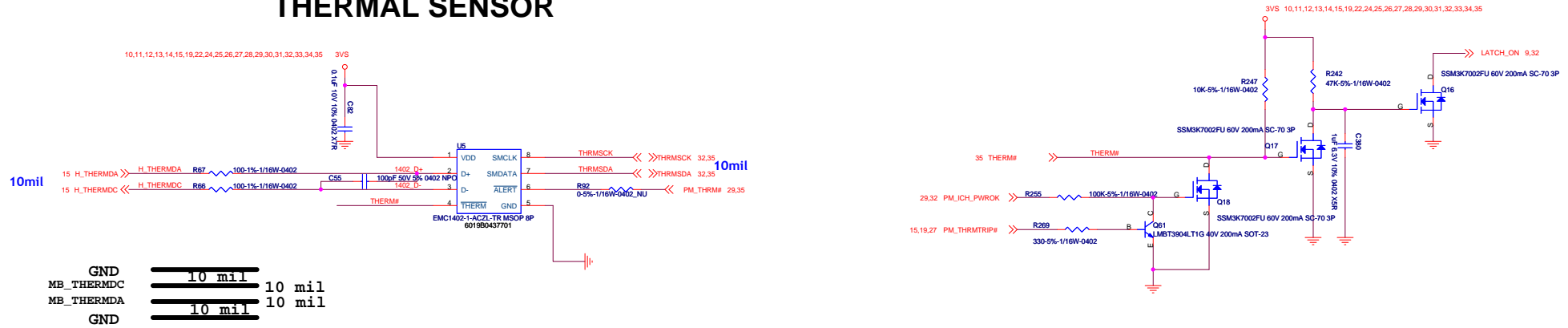


Should be connect to ICH9 and Cantiga without T-ing(no stub)

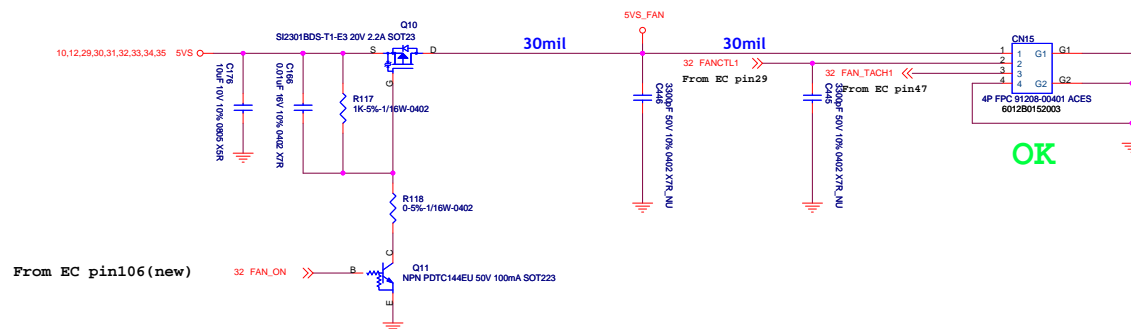


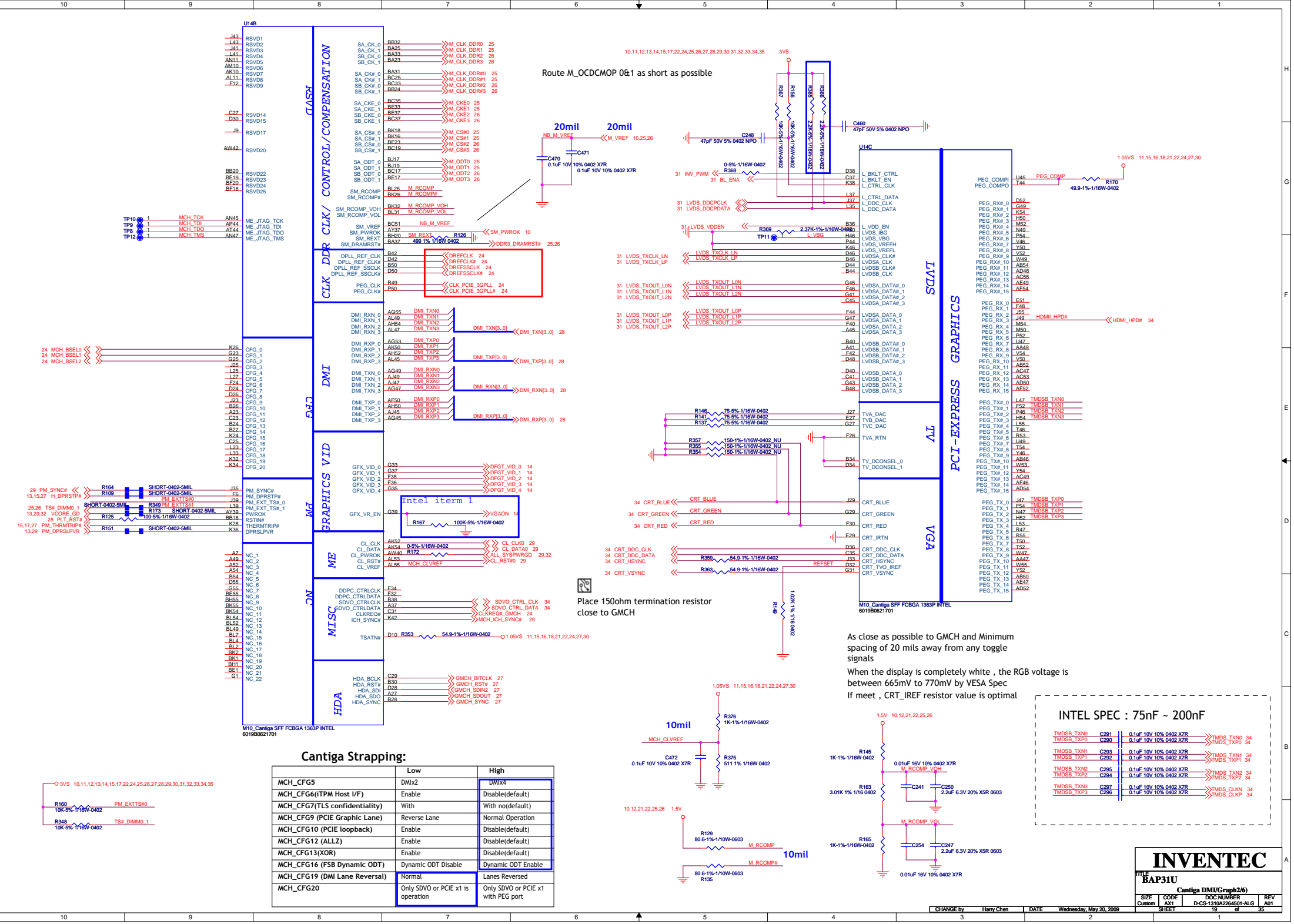
H_PWRGD rise time :
Max : 15ns

THERMAL SENSOR



Fan control





Cantiga Strapping:		
	Low	High
MCH_CFG5	DMIx2	DMIx4
MCH_CFG6(I7PM Host I/F)	Enable	Disable(default)
MCH_CFG7(TLS confidentiality)	With	With no(default)
MCH_CFG9(GMCH Graphic Lane)	Reverse Lane	Normal Operation
MCH_CFG10 (PCIe loopback)	Enable	Disable(default)
MCH_CFG12 (ALLZ)	Enable	Disable(default)
MCH_CFG13(XOR)	Enable	Disable(default)
MCH_CFG16 (FSB Dynamic ODT)	Dynamic ODT Disable	Dynamic ODT Enable
MCH_CFG19 (DMI Lane Reversal)	Normal	Lanes Reversed
MCH_CFG20	Only SDVO or PCIe x1 is operation	Only SDVO or PCIe x1 with PEG port

INTEL SPEC : 75nF - 200nF			
TMDSB_TXN0	C291	0.1uF 10V 10% 0402 X7R	TMDSB_TXN0 34
TMDSB_TXP0	C290	0.1uF 10V 10% 0402 X7R	TMDSB_TXP0 34
TMDSB_TXN1	C293	0.1uF 10V 10% 0402 X7R	TMDSB_TXN1 34
TMDSB_TXP1	C292	0.1uF 10V 10% 0402 X7R	TMDSB_TXP1 34
TMDSB_TXN2	C294	0.1uF 10V 10% 0402 X7R	TMDSB_TXN2 34
TMDSB_TXP2	C295	0.1uF 10V 10% 0402 X7R	TMDSB_TXP2 34
TMDSB_TXN3	C297	0.1uF 10V 10% 0402 X7R	TMDSB_TXN3 34
TMDSB_TXP3	C296	0.1uF 10V 10% 0402 X7R	TMDSB_TXP3 34

INVENTEC

FILE

BAP31U

SIZE

CODE

SHEET

AX1

AX2

AX3

DOC NUMBER

D-CB-1310A284001-ALG

REV

A01

19

of

35

Cantiga DMI/Graph2(6)

CHANGE by

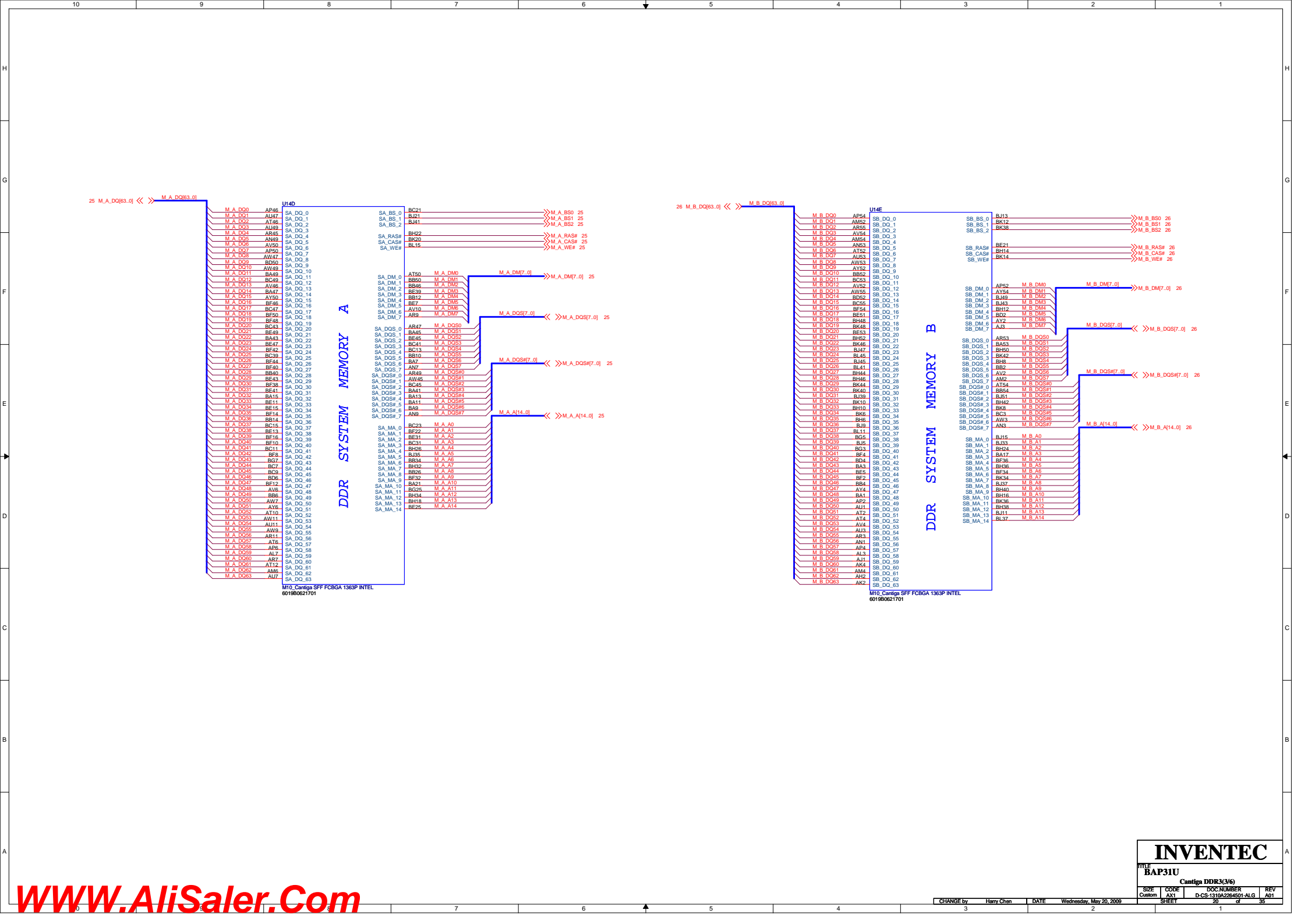
Harry Chen

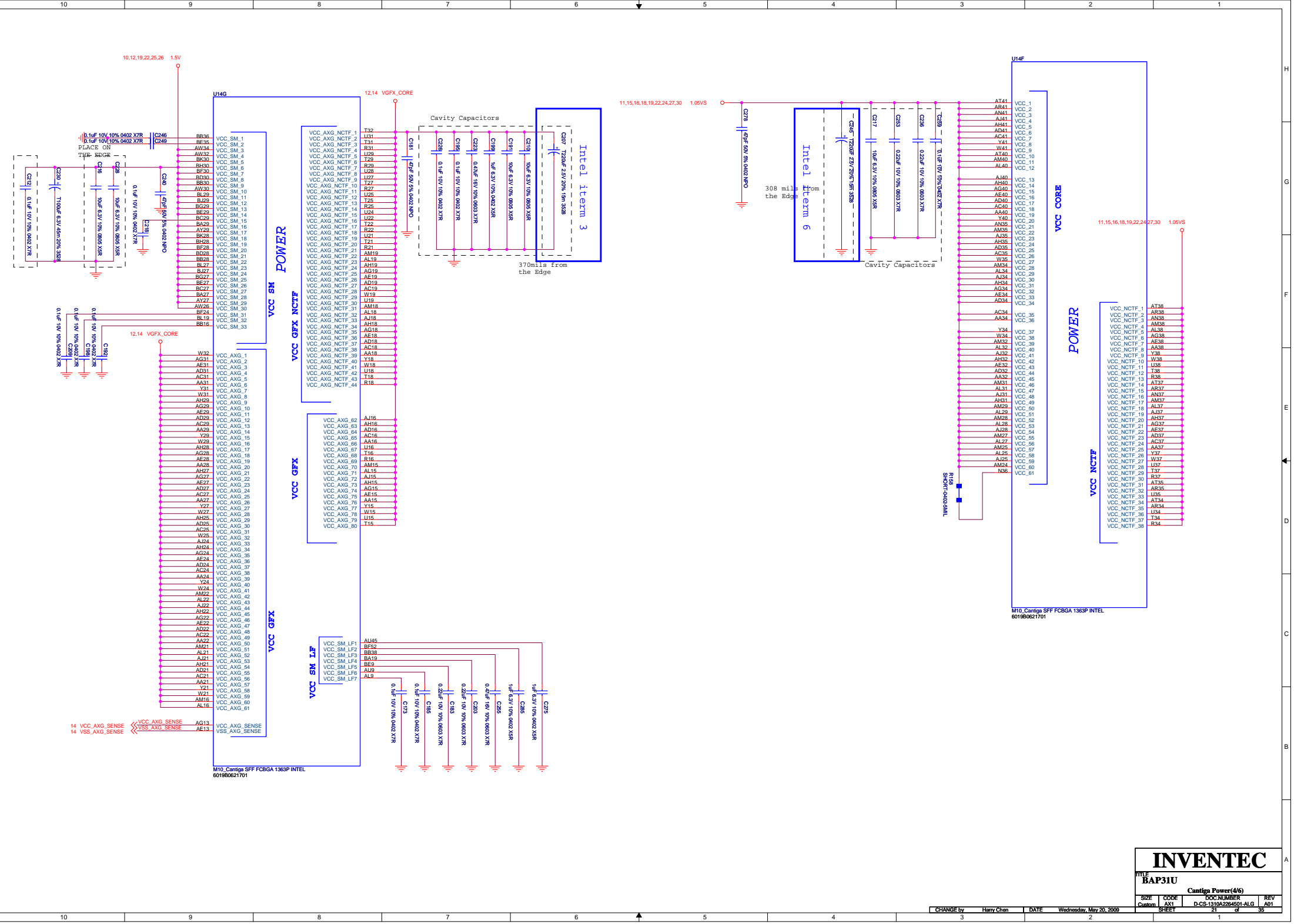
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Wednesday, May 20, 2008

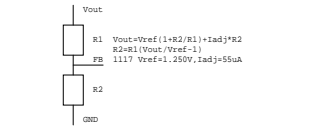
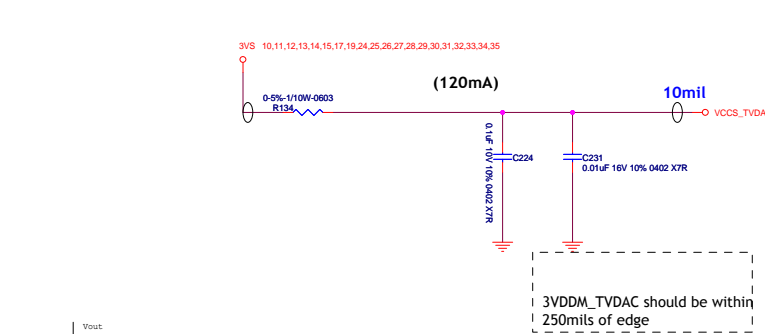
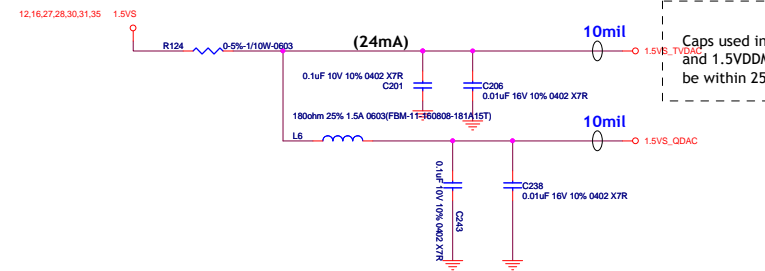
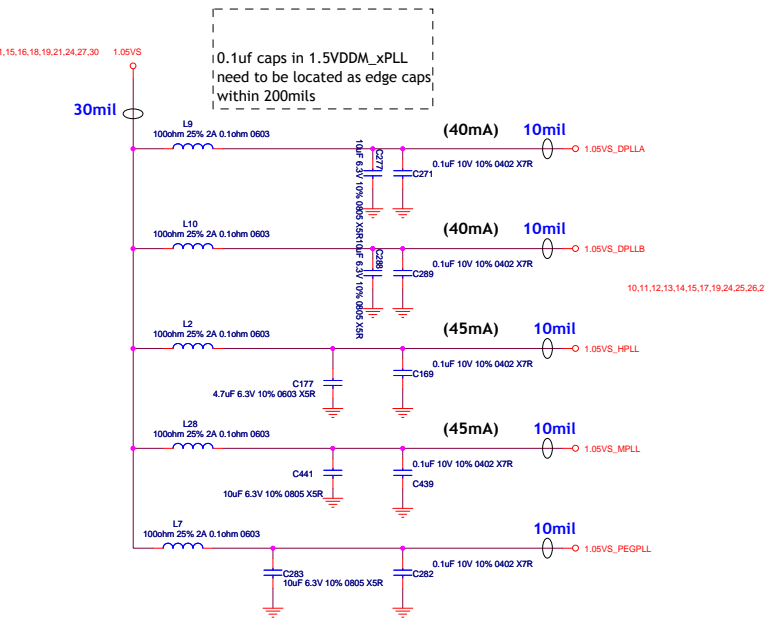
Place 150ohm termination resistor close to GMCH

As close as possible to GMCH and Minimum spacing of 20 mils away from any toggle signals
When the display is completely white , the RGB voltage is between 665mV to 770mV by VESA Spec
If meet , CRT_IREF resistor value is optimal

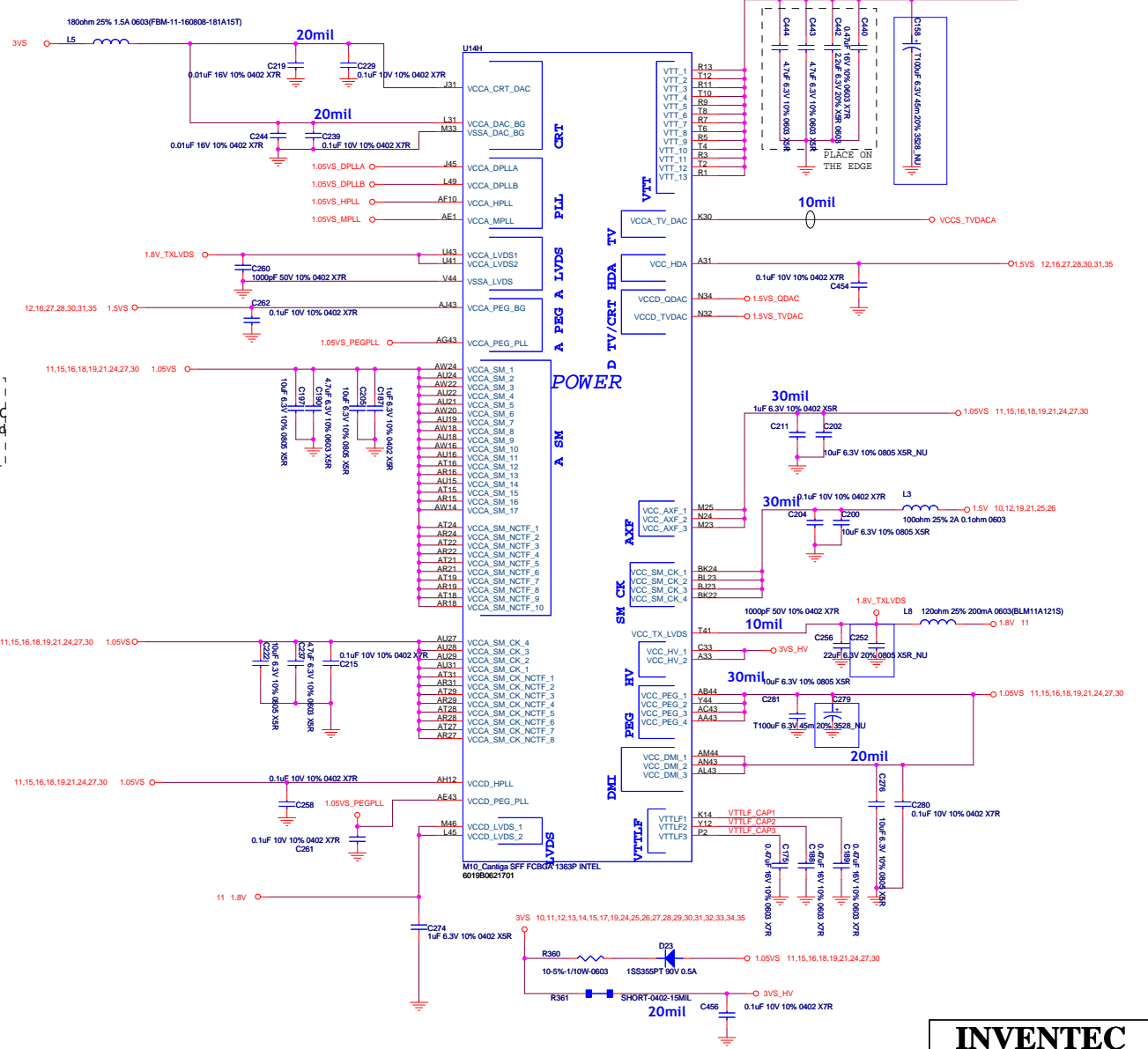




0.1uF caps in 1.5VDDM_xPLL need to be located as edge caps within 200mils

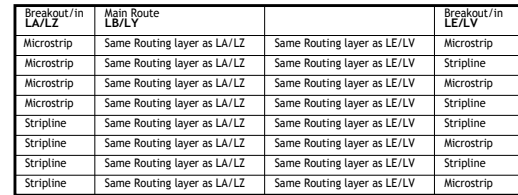


WWW.AliSaler.Com

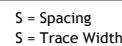


INVENTEC				
BAP31U				
Cantiga Power(5/6)				
SIDE	CODE	DOC NUMBER	REV	
Custom	A11	D-C3-1310A2294591-ALG	A01	
SHEET 22 of 35				

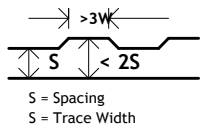
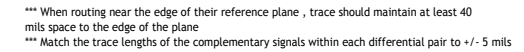
CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009
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*** Match the trace lengths of the complementary signals within each differential pair to ± 5 mils

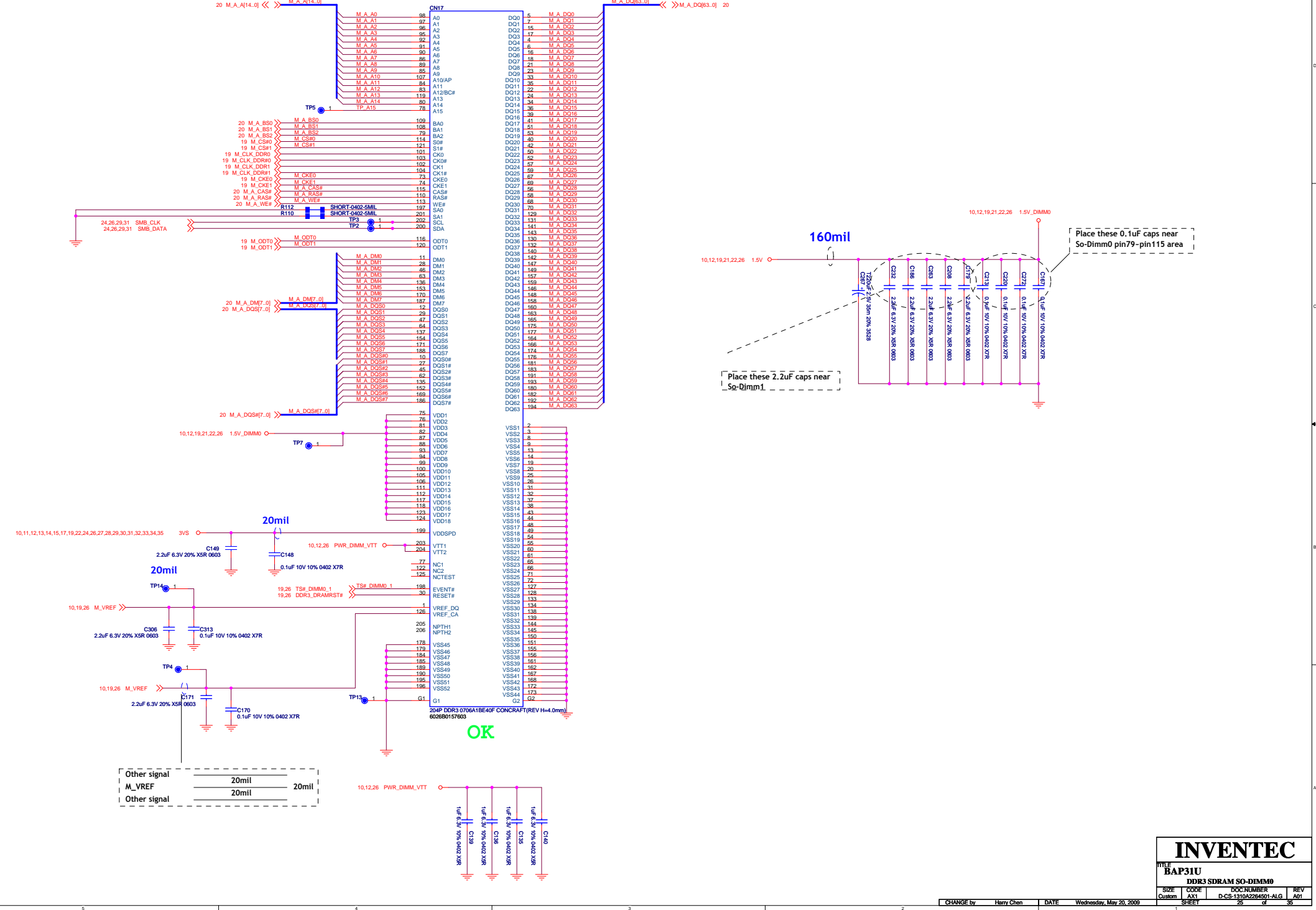


Block diagram of the GMCH Express/Mini Card interface. The GMCH side has Tx and Rx ports. Tx connects to LA, which connects to LB. LB connects to a series combination of a capacitor and an inductor, which then connects to LC. LC connects to the Rx port of the Express/Mini Card. Rx connects to LZ, which connects to LY. LY connects to the Tx port of the Express/Mini Card.



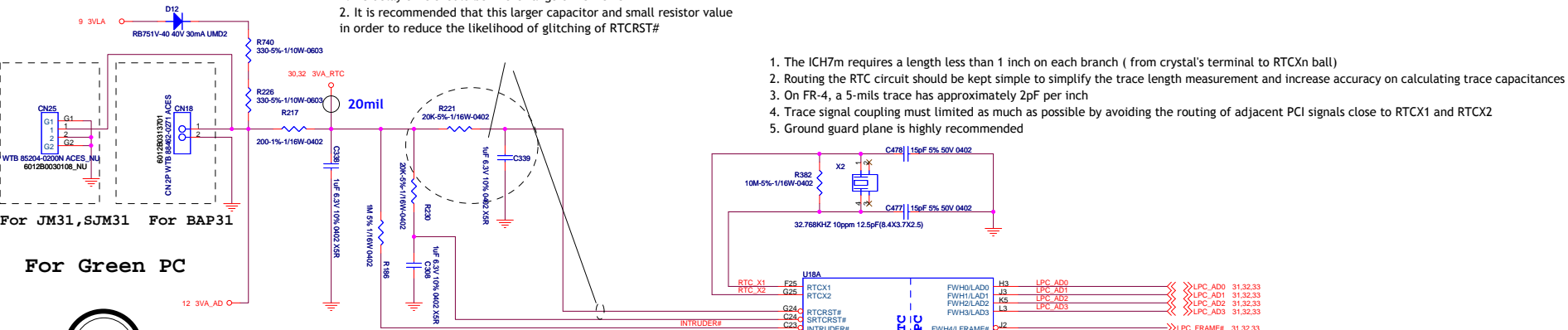
TITLE BAP31U			
Cantiga Ground(6/6)			
SIZE Custom	CODE AX1	DOC NUMBER D-CS-1310A2264501-ALG	REV A01
SHEET		23	of 35

SO-DIMMO

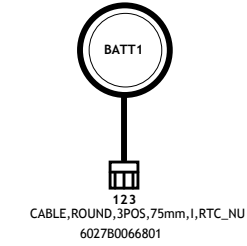


RTC Circuit

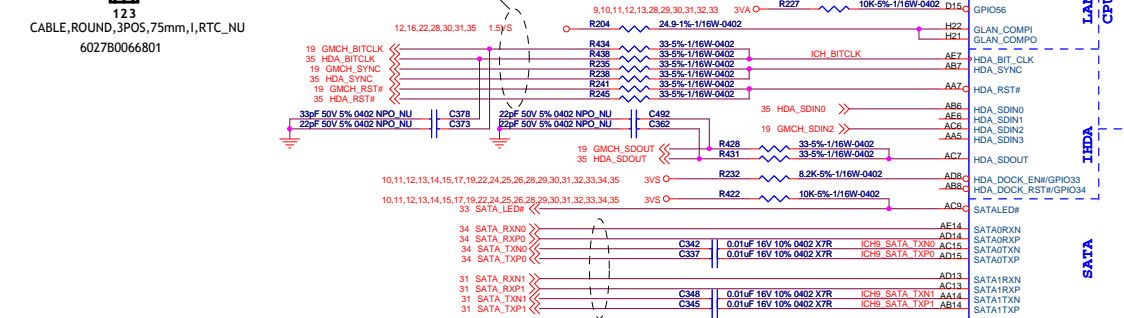
- 1. RC delay time should be in the range of 18-25ms
- 2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#



For Green PC



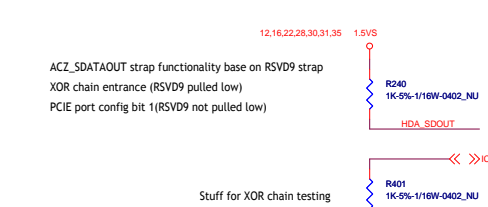
Place all series resistors 0.6 to 2.6 inches from the ICH9



Distance between the ICH9-M and cap on the "P" signal should be identical distance between the ICH9-M and cap on the "N" signal for same pair.

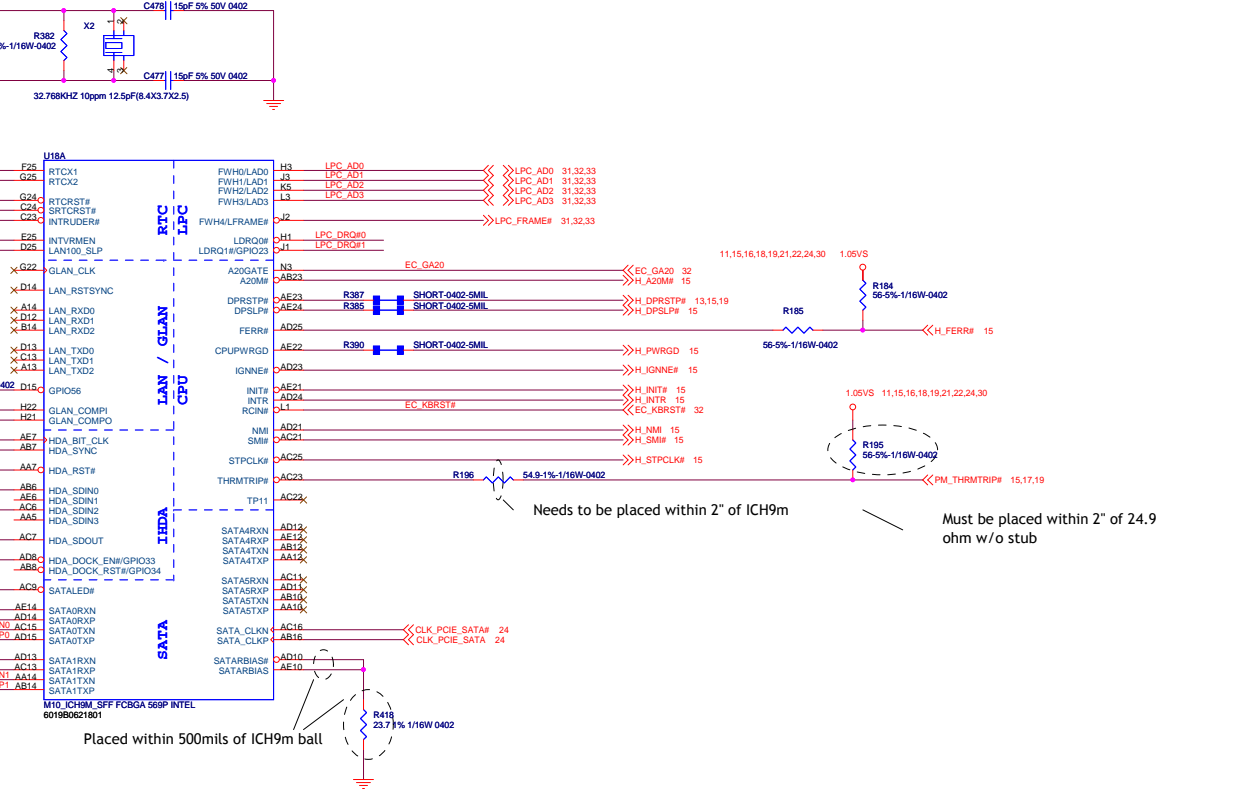
ICH9M internal VR enable strap		
	Enable	Disable
INTVRMEN	1(Default)	0

Internal VRM enabled for VccSus1_05, VccSus1_5, VccCL1_5, VccLAN1_05 and VccCL1_05



XOR Chain Entrance Strap - to be updated	
ICH_TP1	Description
0	0
0	1
1	0
1	1

- 1. The ICH7m requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
- 2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
- 3. On FR-4, a 5-mils trace has approximately 2pF per inch
- 4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
- 5. Ground guard plane is highly recommended



Placed within 500mils of ICH9m ball

Short pins AG1 and AG2 at the package



By Tony

INVENTEC

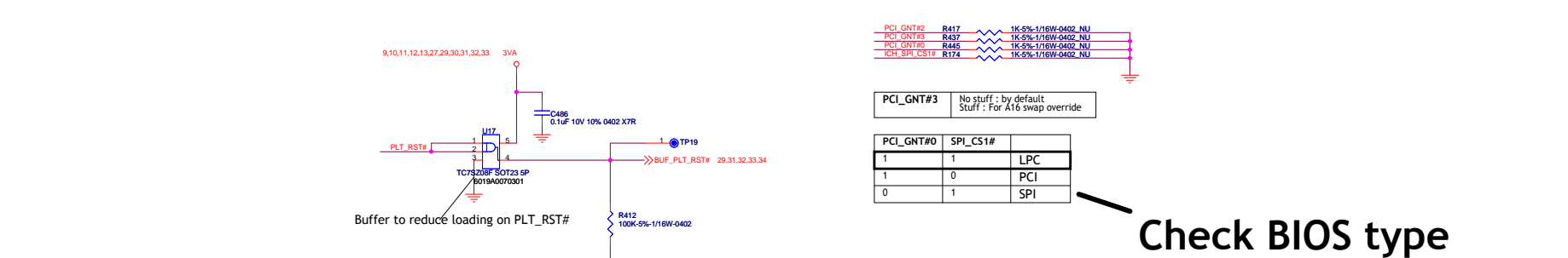
FILE BAP3IU

ICH9M CPU/IDE/SATA(1/4)

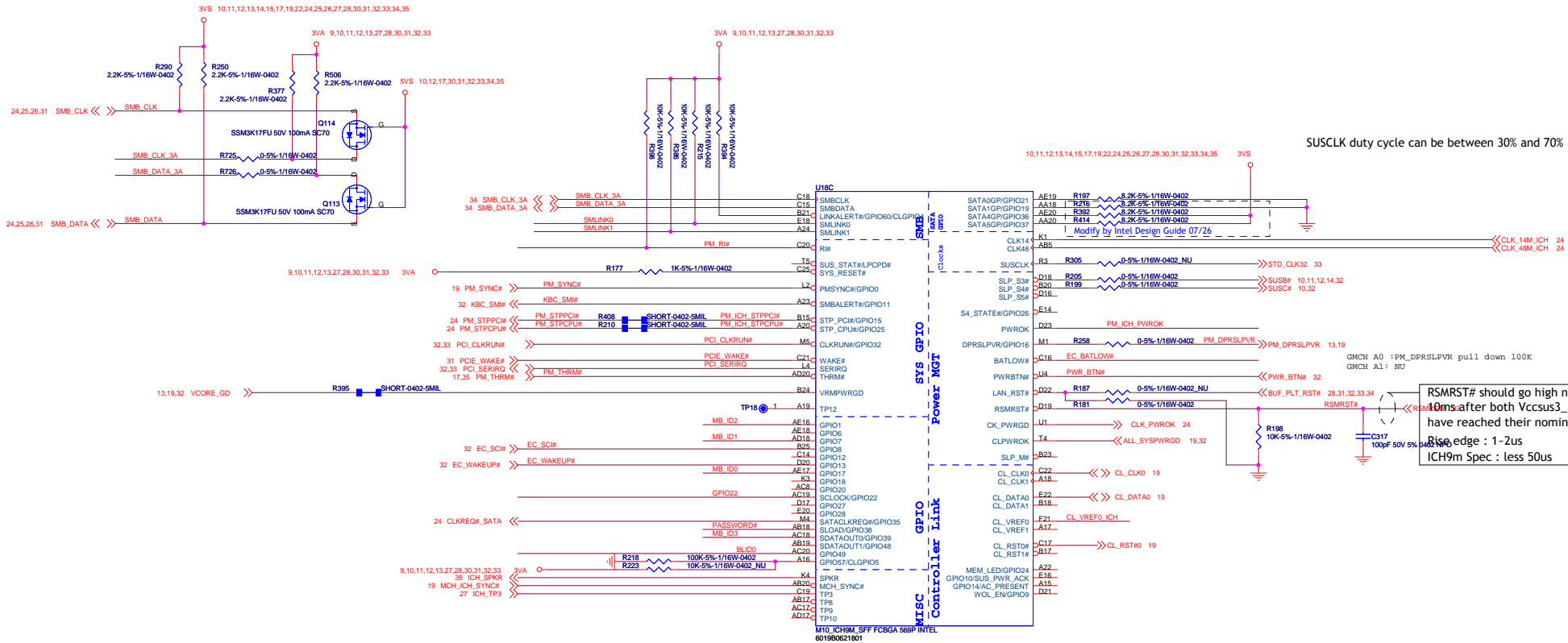
SIZE CODE DOC NUMBER REV

Custom AXI D-CS-1310A2284501-ALG A01

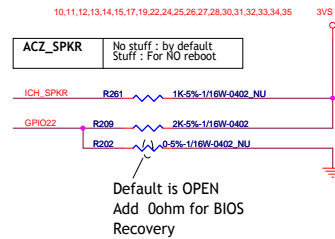
SHEET 27 of 35



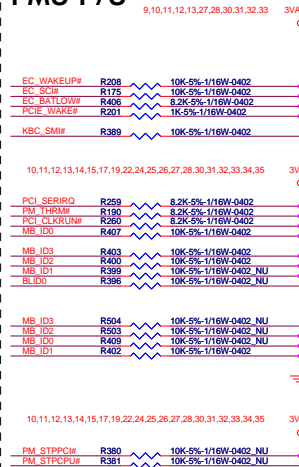
INVENTEC			
TITLE BAP31U			
ICH9M PCI/PCIE/DMI/USB(2/4)			
SIZE Custom	CODE AX1	DOC NUMBER D-CS-1310A2264501-ALG	REV A01
SHEET		28	of 35



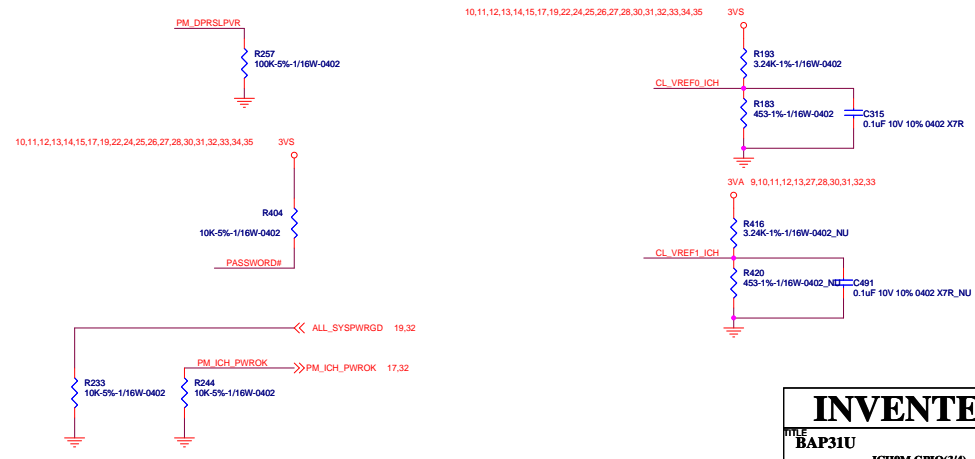
ICH9m strap



PMU P/U



BIOS ID setting				
Project	MB_ID3	MB_ID2	MB_ID1	MB_ID0
JM31 (UMA)	1	1	1	1
SJM31 (UMA)	1	1	1	0
BAP31 (UMA)	1	1	0	1
	1	1	0	0
	1	0	1	1
	1	0	1	0
	1	0	0	1
	1	0	0	0
	0	1	1	1
	0	1	1	0
	0	1	0	1
	0	1	0	0
	0	0	1	1
	0	0	1	0
	0	0	0	1
	0	0	0	0



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FILE BAP31U ICH9M GPIO(3/4)

SIZE Custom DOC NUMBER REV
AX1 D-CS-1310A284501-ALG A01
SHEET 29 of 35

30P LVDS 50373-03001-001 AECES 6012B031301

INVERT CONTROL

30P LVDS 50373-03001-001 AECES 6012B031301

OK

3V 9,10,11,12,13,27,28,29,30,32,33

19 BL_ENA

32 BL_LID#

U13

R342

100K 1% 1/6W 0402

TC7S208F SOT23 5P

6019A0070301

BACKLIGHT

The diagram illustrates the internal wiring of a SATA to SATA II adapter. It shows the connection between the SATA I side (left) and the SATA II side (right). Key components and connections include:

- Power and Ground:** A 5V power source is connected to the SATA I side via a 561 resistor. Ground connections are shown on both sides.
- Signal Traces:** Traces for SATA I signals (TXP1, TXN1, RXN1, RXP1) and SATA II signals (S1-S7, P1-P15) are shown. A large circle highlights a specific signal trace area.
- Capacitors:** Two capacitors, C499 and C498, are connected to the TXN1 and RXN1 signals respectively. Their values are 0.01uF 16V 10% 0402 X7R.
- Resistors:** A 561 resistor is connected to the 5V power source. A 60mil trace is shown for the signal path.
- Termination:** A 100ohm termination resistor is connected to the TXN1 signal.
- Labels:** The diagram includes labels for "CAP. NEAR CON.", "SHORT-0805-40MIL", and "60mil".

[illegible]

CIE Mini Card for 3G

29 PCIE_WAKE#
33 BT_PRI
34 WLAN_ACT
24 CLK_PCIE_MINICARD2#
24 CLK_PCIE_MINICARD2

28 PCIE_RXN2
28 PCIE_RXP2

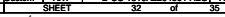
28 PCIE_TXN2
28 PCIE_TXP2

3G VCC

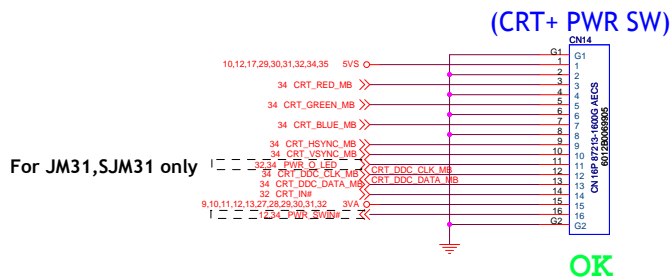
MINI PCIE SZP 60602-1021 BELLWETHER H-S 32mm
6026B0172701

On Chip 5V to 3.3V regulator. No external regulator required
On-Chip power MOSFETs for supplying flash media card power.

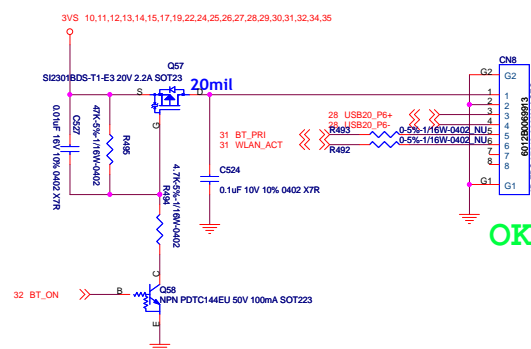
TITLE BAP31U			
LCD CNN & WLAN & 3G			
SIZE Custom	CODE AX1	DOC.NUMBER D-CS-1310A2264501-ALG	REV A01
SHEET		31	of 35



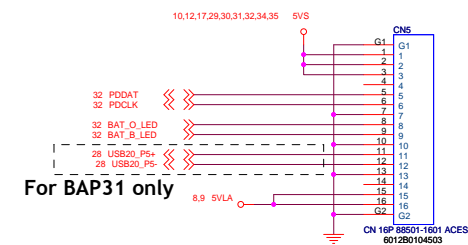
VGA Board CN



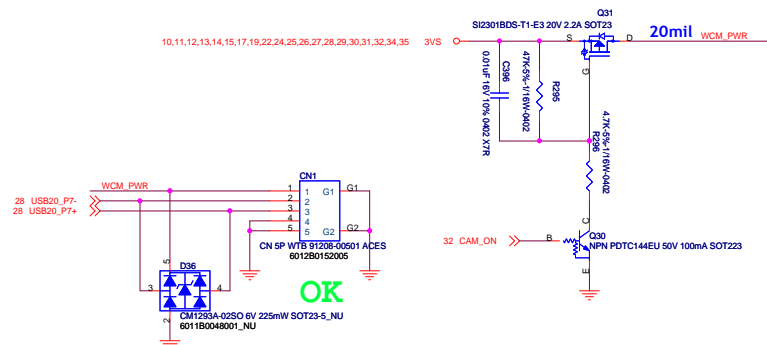
Bluetooth CON.



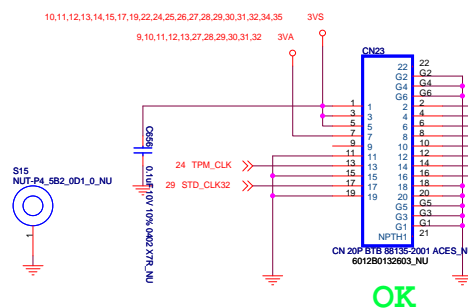
MB(GP) TO GP/B



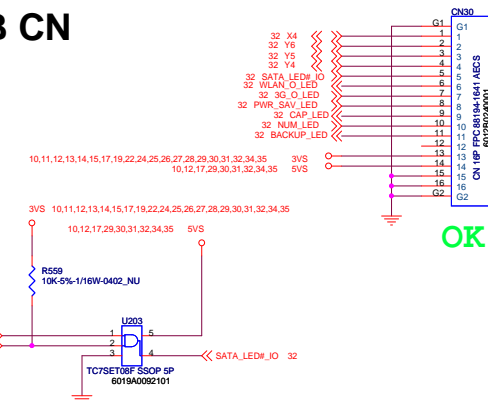
WEB Cam.



TPM CN

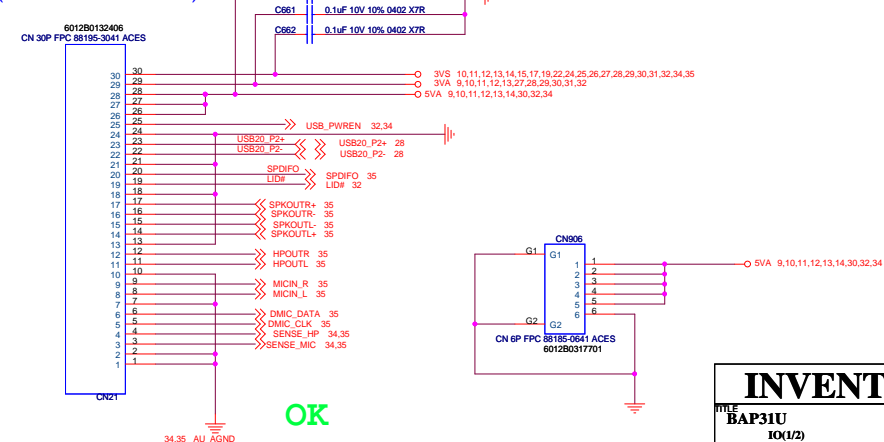


SW/B CN



AUDIO Board CN

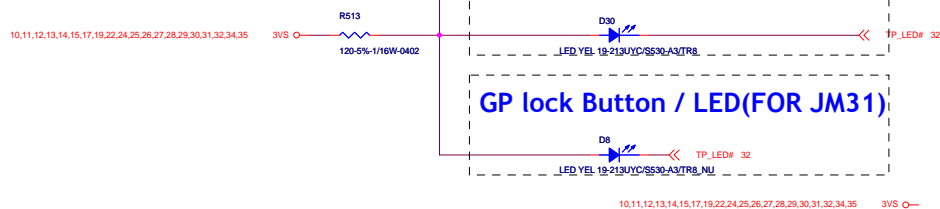
(Audio JACK+1USB)



GP lock Button / LED(FOR SJM31)

GP lock Button / LED(FOR BAP31)

GP lock Button / LED(FOR JM31)



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FILE BAP31U

IO(I/2)

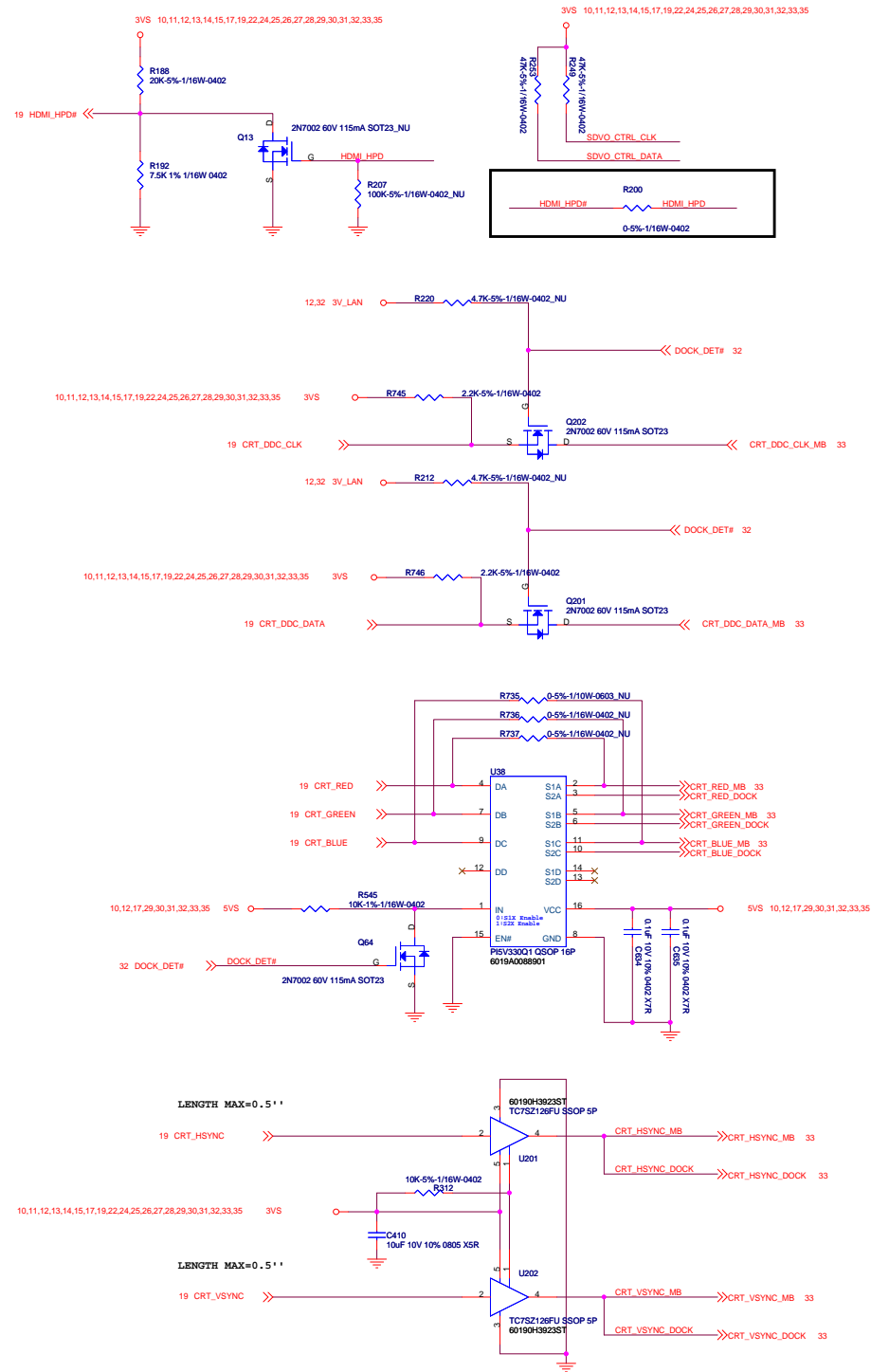
SIZE CODE DOC NUMBER REV

Custom AXI D-GS-1310A2284501-ALG A01

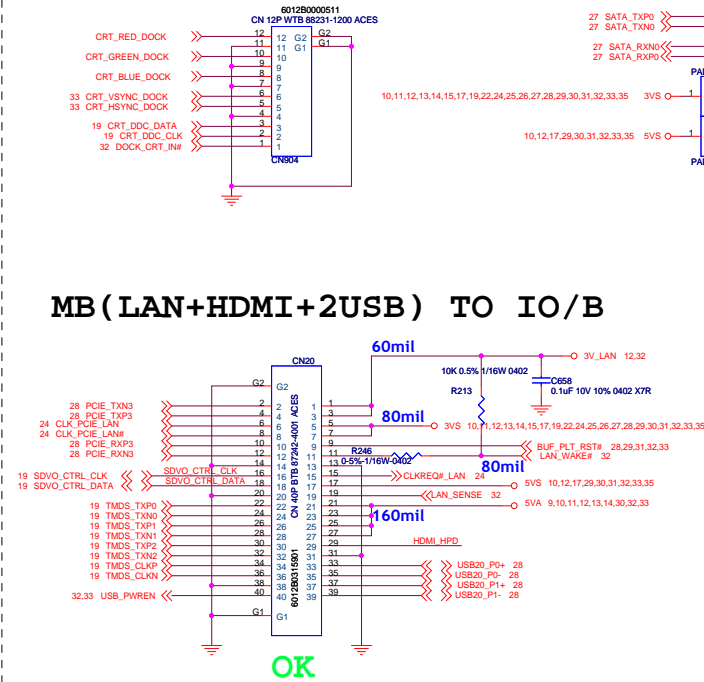
CHANGE by Henry Chen DATE Wednesday, May 20, 2009

SECRET

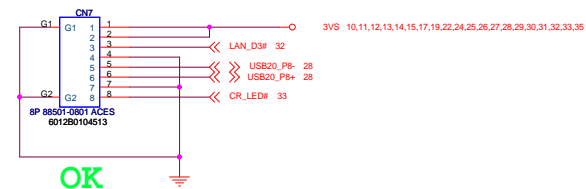
For BAP31 IO/B



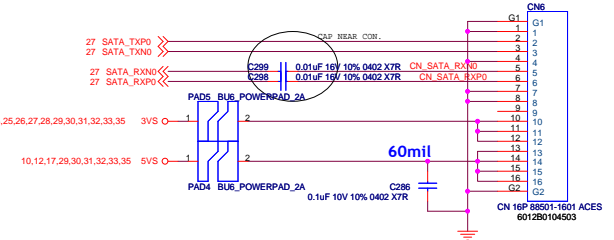
MB(USB) TO IO/B



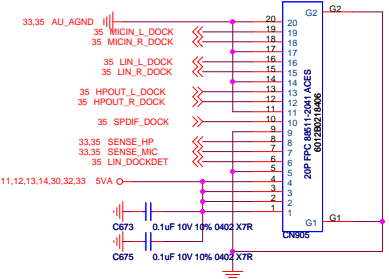
MB(CardReader) TO IO/B



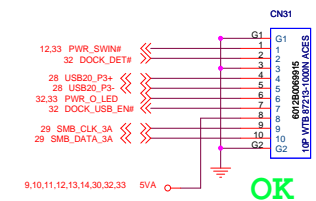
MB(SSD) TO IO/B



MB(AUDIO) TO IO/B



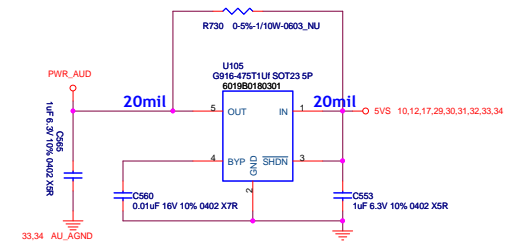
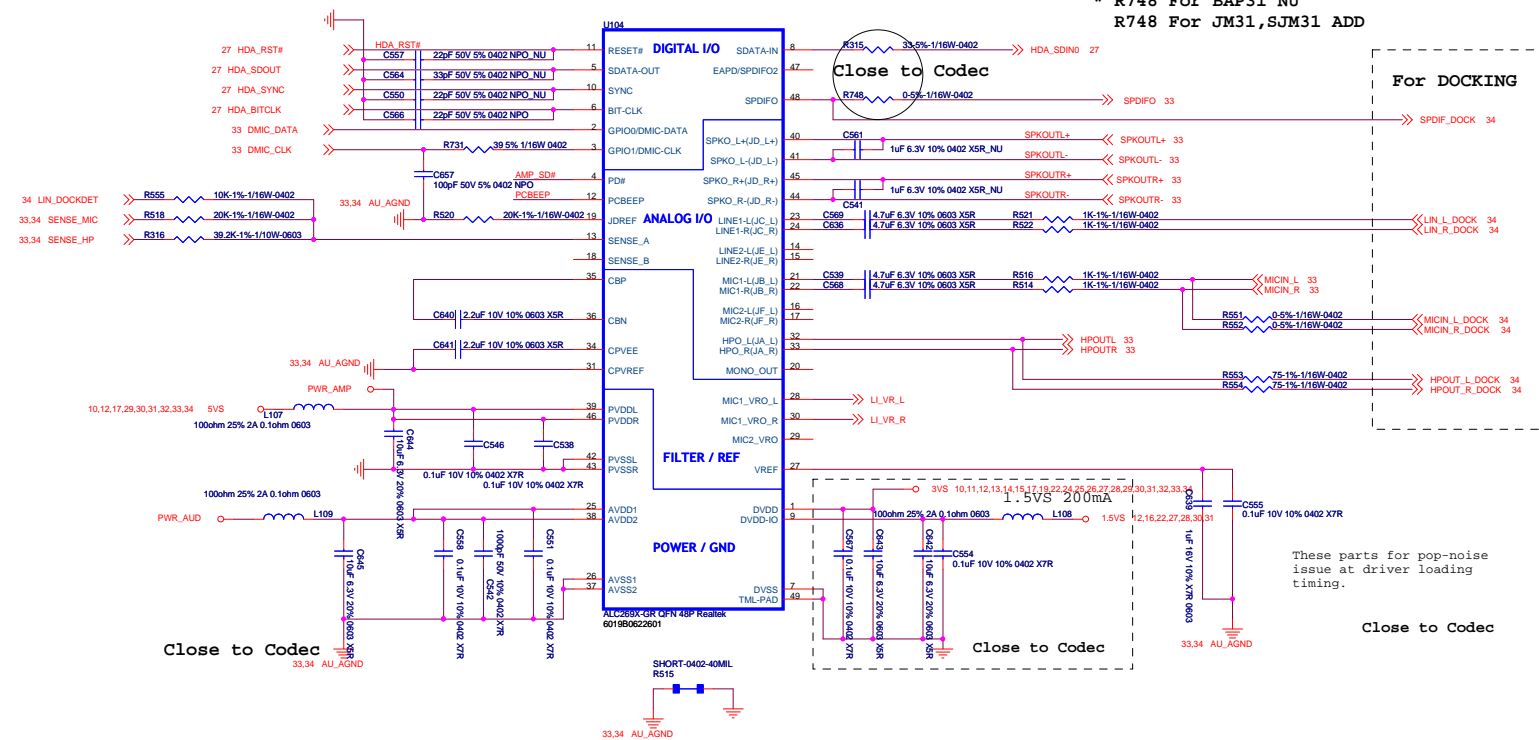
MB(USB) TO IO/B



INVENTEC

SIZE	CODE	DOC NUMBER	REV
Custom	AX1	D-GS-1310A2284501-ALG	A01
SECRET			

CHANGE by: Harry Chen DATE: Wednesday, May 20, 2009



Please check the layout location with EMC.

